DETAILED ACTION

1. Claims 1, 5-16, 18-19, and 24-49 have been presented for examination.

Claims 2-4, 17, and 20-23 have been cancelled.

Examiners Amendment

2. An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

Authorization for this examiner's amendment was given in a telephone interview with J. Matthew Zigmant, 44005, on 9 December 2009.

The application has been amended as follows:

i) Amend claim 16:

A method as claimed in claim 15, further comprising the step of: connecting the software debugger to the inter-process communications protocol connection.

ii) Amend claim 38:

A method for simulating a system which comprises a software element and first and second hardware components, the software element being for execution on the second hardware component, and the first and second hardware components being operable to interact with one another, the method comprising:

simulating operation of the first hardware component in a first simulation;

simulating the software element and the second hardware component in a second simulation;

receiving a variable synchronization parameter; wherein the variable synchronization parameter may be dynamically varied while simulating the software element and the second hardware component in the second simulation; and

running the second ~~software~~ simulation asynchronously with, and ahead of, the first ~~software~~ simulation, wherein the second ~~software~~ simulation advances at most by a number of processor clock cycles set in the variable synchronization parameter before the first ~~software~~ simulation advances by a clock cycle,

wherein the first simulation and the second simulation are implemented in separate processing threads.

iii) Amend claim 39:

The method of claim 38, wherein the variable synchronization parameter limits a maximum number of processor clock periods of the second simulation per period of a reference clock of the host machine.

iv) Amend claim 44:

A method for controlling a simulation of a system using a software debugger, wherein the system comprises a software element, and first and second hardware components, the software element being for execution on the second hardware component and the first and second hardware components being operable to interact with one another, the method comprising the steps of:

simulating the first hardware component in a first simulation;

simulating the second hardware component in a second simulation;

receiving a variable synchronization parameter, wherein the variable synchronization parameter may be dynamically varied while running the second simulation;

running the second simulation asynchronously with, and ahead of, the first simulation, wherein the second simulation advances at most by a number of processor clock cycles set in the variable synchronization parameter before the first simulation advances by a clock cycle;

performing operations in the first simulation to set up an inter-process communications protocol connection; and

controlling the first simulation from the software debugger using the inter-process communications protocol.

Allowable Subject Matter

3. The following is an examiner's statement of reasons for allowance: claims 1, 5-16, 18-19, and 24-49 are considered allowable since when reading the claims in light of the specification, none of the references of record alone or in combination disclose or suggest the combination of limitations specified in the independent claims, specifically:

The recitation with respect to claims 1, 15, 29, 38, and 44 of receiving a variable synchronization parameter, wherein the variable synchronization parameter may be dynamically varied while running the second simulation; and running the second simulation asynchronously with, and ahead of, the first simulation, wherein the

second simulation advances at most by a number of processor clock cycles set in the variable synchronization parameter before the first simulation advances by a clock cycle. Claim 29 references a reference clock parameter which is defined in the same manner. More specifically the dynamic nature of the synchronization parameter is the defining aspect of the claim language as dynamically selectable refers to the variable nature of the parameter.

The claims are rendered statutory since they recite method for simulating or controlling simulation through the use of a computer and further that the simulations including the simulating of a hardware component. As per page 5 of the specification the simulation aspect of the claims utilizes a HDL which require a computer for both design and implementation.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

4. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Saif A. Alhija whose telephone number is (571) 272-8635. The examiner can normally be reached on M-F, 11:00-7:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kamini Shah can be reached on (571) 272-2279. The fax phone number for the organization where this application or proceeding is assigned is (571) 273-8300.

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SAA

/Kamini S Shah/
Supervisory Patent Examiner, Art Unit 2128

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